AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (previously presented) A fractional-N synthesizer with programmable output phase comprising:

a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal, said phase locked loop including a frequency divider;

a synchronization circuit responsive to said input reference signal for generating synchronization pulses at integer multiples of M periods of said input reference signal;

an interpolator responsive to F and M, where F is a fractional value and M is the modulus, to provide to said frequency divider an output which is a fractional value equal to, on average, an input fraction F/M; and

a phase adjustment circuit responsive to said synchronization circuit for varying the phase of said output signal with respect to said input reference signal.

2. (previously presented) The fractional-N synthesizer of claim 1 in which said phase adjustment circuit includes a switching circuit for selectively applying said fractional value and a modified fractional value to said interpolator to define a predetermined phase relationship between said output signal and said input reference signal.

3. (original) The fractional-N synthesizer of claim 2 in which said switching circuit includes an adder circuit for adding said fraction value and a predetermined phase adjustment value to define said modified fractional value.

4. (original) The fractional-N synthesizer of claim 3 in which said switching circuit includes a multiplexer configured to select said modified fractional value or said fractional value for one or more reference cycles.

5. (original) The fractional-N synthesizer of claim 3 in which said fractional value is offset by a phase word to define said modified fractional value.

6. (previously presented) The fractional-N synthesizer of claim 5 in which said phase word has a size in the range of 0 to M–1.

7. (previously presented) A fractional-N synthesizer with programmable output phase comprising:

a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal, said phase locked loop including a frequency divider;

a synchronization circuit responsive to said input reference signal for generating synchronization pulses at integer multiples of M periods of said input reference signal;

a phase register including a predetermined phase adjustment value; and

an interpolator responsive to F and M, where F is the fractional value, and M is the modulus, and said phase register, to provide to said frequency divider an output which is a

fractional value equal to, on average, said input fraction, wherein an enable signal applied to said synchronization circuit resets said interpolator with said predetermined phase adjustment value to vary the phase of said output signal with respect to said input reference signal.

8. (original) A fractional-N synthesizer with programmable output phase comprising:

a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal, said phase locked loop including a frequency divider;

a phase adjustment circuit responsive to said input reference signal, an enable signal, a fraction (F), and a predetermined phase value, and a modulus (M), said phase adjustment circuit configured to generate a modified phase adjustment value; and

an interpolator responsive to said phase adjustment circuit to provide to said frequency divider an output which is a fractional value equal to, on average, an input fraction F/M varied by said modified phase adjustment value to vary the phase of said output signal with respect to said input reference signal.

9. (original) The fractional-N synthesizer of claim 8 in which said phase adjustment circuit includes a modulo-M counter for counting a predetermined number of reference clock cycles.

10. (original) The fractional-N synthesizer of claim 9 in which said phase adjustment circuit includes a modulo-M multiplier responsive to said modulo-M counter and an input

fraction for multiplying the number of reference clock edge edges counted by the input fraction by said input fraction.

11. (original) The fractional-N synthesizer of claim 10 in which said phase adjustment circuit further includes an additional modulo-M adder responsive to said modulo-M multiplier and a predetermined phase adjustment value for adding the result of said modulo-M multiplier and said predetermined phase adjustment value to produce said modified phase adjustment value.

12. (previously presented) A fractional-N synthesizer with programmable output phase comprising:

a phase locked loop having an output signal whose frequency is a fractional multiple of an input reference signal, said phase locked loop including a frequency divider;

a synchronization circuit responsive to said input reference signal for generating synchronization pulses at integer multiples of M periods of said input reference signal;

an interpolator responsive to F and M, where F is the fractional value and M is the modulus, to provide to said frequency divider an output which is a fractional value equal to, on average, said input fraction; and

a phase adjustment circuit responsive to said synchronization circuit for varying the phase of said output signal with respect to said input reference signal, said phase adjustment circuit including a switching circuit for selectively applying said fractional value and a modified

fractional value to said interpolator to define a predetermined phase relationship between said output signal and said input reference signal.

13. (currently amended) A method of varying the phase of the output signal with respect to the input reference signal of a fractional-N synthesizer, the method comprising the steps of:

tracking an accumulated fractional phase;

scaling the accumulated fractional phase by a predetermined phase value; and

loading the predetermined phase value into an interpolator and providing an output from the interpolator to a frequency divider to define a predetermined output frequency and phase.

14. (currently amended) A method of varying the phase of the output signal with respect to the input reference signal of a fractional-N synthesizer, the method comprising:

generating a synchronization pulse at integer multiples of periods of the input reference signal; and

selectively applying a fractional value and a modified fractional value to an interpolator of said fractional-N synthesizer to define a predetermined phase relationship between said output signal and said input reference signal.

15. (previously presented) A method of varying the phase of the output signal with respect to the input signal of a fractional-N synthesizer, the method comprising:

generating a synchronization pulse at integer multiples of periods of the input

reference signal;

generating a predetermined phase adjustment value; and

generating an enable signal to reset an interpolator of said fractional-N synthesizer with said predetermined phase to vary the phase of said output signal with respect to the phase of said input reference signal.